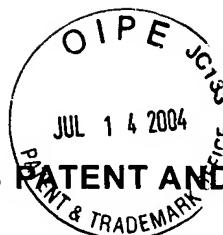


EV372456478



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No. .... 10/007,300  
Filing Date ..... November 8, 2001  
Inventor ..... Keiji Jono et al.  
Assignee ..... KMT Semiconductor, LTD  
Group Art Unit ..... 2811  
Examiner ..... Thien F. Than  
Attorney Docket No. ..... KM1-003  
Customer No. ..... 021567  
Title: Trench-Isolated Transistors, Trench Isolation Structures, Memory Cells,  
and DRAMs

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

References -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. Copies of the cited prior art references are attached. No admission is made regarding whether all the listed references are prior art.

Respectfully submitted,

Dated: 7-14-04

By:   
Mark S. Matkin  
Reg. No. 32,268

07/16/2004 SSITHIB1 00000127 10007300

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Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. KM1-003		SERIAL NO. 10/007,300	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT: Keiji Jono et al.			
				FILING DATE November 8, 2001		GROUP 2811	
U.S. PATENT DOCUMENTS							
*Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,342,428 B1	01/20/02	Zheng et al.			
	AB	6,380,095 B1	04/30/02	Liu et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes
	AJ						
	AK						
	AL						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AM						
	AN						
	AO						
EXAMINER		DATE CONSIDERED					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							